

## BIAS TEMPERATURE INSTABILITY FOR DEVICES AND CIRCUITS%0A

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### **Bias Temperature Instability for Devices and Circuits**

This book provides a single-source reference to one of the more challenging reliability issues plaguing modern semiconductor technologies, negative bias temperature instability. Readers will benefit from state-of-the art coverage of research in topics such as time dependent defect spectroscopy, anomalous defect behavior, stochastic modeling with additional metastable states, multiphonon theory, compact modeling with RC ladders and implications on device reliability and lifetime.

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Enables readers to understand and model negative bias temperature instability, with an emphasis on dynamics Includes coverage of DC vs. AC stress, duty factor dependence and bias dependence Explains time dependent defect spectroscopy, as a measurement method that operates on nanoscale MOSFETs

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**Negative Bias Temperature Instability NBTI IEEE**

Negative bias temperature instability occurs mainly in p-channel MOS devices Either negative gate voltages or elevated temperatures can produce NBTI, but a stronger and faster effect is produced by their combined action Oxide electric fields typically below 6 MV/cm Stress temperatures: 100 - 250 C Drain current, transconductance, and off current decrease Absolute threshold voltage <http://yorkgaming.co/Negative-Bias-Temperature-Instability--NBTI--IEEE.pdf>

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